

# CCD image sensors



S11071/S10420-01 series

## Improved etaloning characteristics, High-speed type and low noise type available

The S11071/S10420-01 series are back-thinned CCD image sensors designed for spectrometers. Two types consisting of a high-speed type (S11071 series) and low noise type (S10420-01 series) are available with improved etaloning characteristics. The S11071/S10420-01 series offer nearly flat spectral response characteristics with high quantum efficiency from the UV to near infrared region.

### Features

- Improved etaloning characteristics
- High sensitivity over a wide spectral range and nearly flat spectral response characteristics
- High CCD node sensitivity: 8  $\mu\text{V}/\text{e}^-$  (S11071 series)  
6.5  $\mu\text{V}/\text{e}^-$  (S10420-01 series)
- High full well capacity and wide dynamic range (with anti-blooming function)
- Pixel size: 14  $\times$  14  $\mu\text{m}$
- High UV resistance: S10420-1106NU-01/-1106NW-01

### Applications

- Spectrometers, etc.

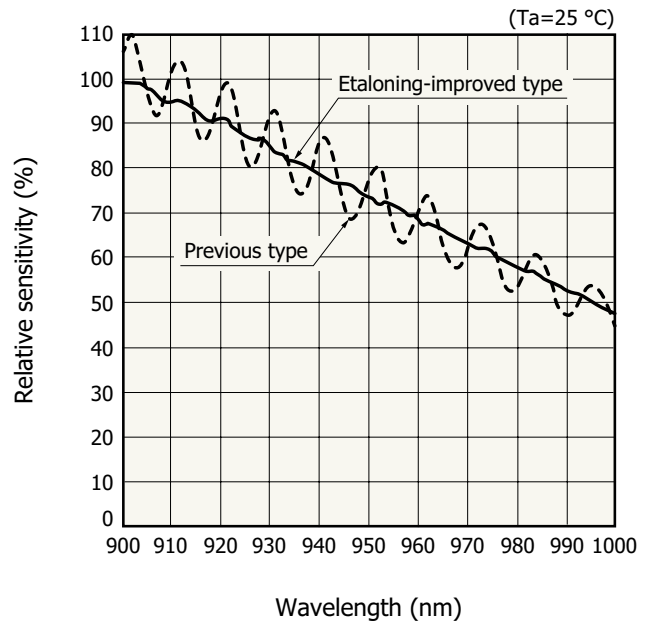
### Selection guide

| Type no.         | Number of total pixels | Number of effective pixels | Image size [mm (H) $\times$ mm (V)] | Readout speed max. (MHz) | Suitable driver circuit |
|------------------|------------------------|----------------------------|-------------------------------------|--------------------------|-------------------------|
| S11071-1004      | 1044 $\times$ 22       | 1024 $\times$ 16           | 14.336 $\times$ 0.224               | 10                       | C11288-01               |
| S11071-1006      | 1044 $\times$ 70       | 1024 $\times$ 64           | 14.336 $\times$ 0.896               |                          |                         |
| S11071-1104      | 2068 $\times$ 22       | 2048 $\times$ 16           | 28.672 $\times$ 0.224               |                          |                         |
| S11071-1106      | 2068 $\times$ 70       | 2048 $\times$ 64           | 28.672 $\times$ 0.896               |                          |                         |
| S10420-1004-01   | 1044 $\times$ 22       | 1024 $\times$ 16           | 14.336 $\times$ 0.224               | 0.5                      | C11287-01               |
| S10420-1006-01   | 1044 $\times$ 70       | 1024 $\times$ 64           | 14.336 $\times$ 0.896               |                          |                         |
| S10420-1104-01   | 2068 $\times$ 22       | 2048 $\times$ 16           | 28.672 $\times$ 0.224               |                          |                         |
| S10420-1106-01   | 2068 $\times$ 70       | 2048 $\times$ 64           | 28.672 $\times$ 0.896               |                          |                         |
| S10420-1106NU-01 |                        |                            |                                     |                          |                         |
| S10420-1106NW-01 |                        |                            |                                     |                          |                         |

**Improved etaloning characteristics**

Etaloning is an interference phenomenon that occurs when the light incident on a CCD repeatedly reflects between the front and back surfaces of the CCD while being attenuated, and causes alternately high and low sensitivity. When long-wavelength light enters a back-thinned CCD, etaloning occurs due to the relationship between the silicon substrate thickness and the absorption length. The S11071/S10420-01 series back-thinned CCDs have achieved a significant improvement in etaloning by using a unique structure that is unlikely to cause interference.

▣ **Etaloning characteristics (typical example)**



KMPDB0284EB

▣ **Structure**

| Parameter              | S11071 series                                     | S10420 series                          |                          |
|------------------------|---|--|--------------------------|
|                        |   | -1004-01/-1006-01<br>-1104-01/-1106-01 | -1106NU-01<br>-1106NW-01 |
| Pixel size (H × V)     | 14 × 14 μm  |  |                          |
| Vertical clock phase   | 2-phase   |  |                          |
| Horizontal clock phase | 4-phase   |  |                          |
| Output circuit         | Two-stage MOSFET source follower                  | One-stage MOSFET source follower       |                          |
| Package                | 24-pin ceramic DIP (refer to dimensional outline) |  |                          |
| Window material        | Quartz glass (resin sealing)*1                    |  | None*2                   |
| Cooling                | Non-cooled  |  |                          |

\*1: Temporary window type (ex: S11071-1106N, S10420-1106N-01) is available upon request.

\*2: Temporary window (borosilicate glass)

➤ Absolute maximum ratings (Ta=25 °C)

| Parameter                               | Symbol                   | Min. | Typ. | Max. | Unit |
|---|--------------------------|------|------|------|------|
| Operating temperature*3                 | Topr                     | -50  | -    | +50  | °C   |
| Storage temperature                     | Tstg                     | -50  | -    | +70  | °C   |
| Output transistor drain voltage         | S11071 series            | -0.5 | -    | +25  | V    |
|   | S10420-01 series         | -0.5 | -    | +30  |      |
| Reset drain voltage                     | VRD                      | -0.5 | -    | +18  | V    |
| Output amplifier return voltage         | Vret                     | -0.5 | -    | +18  | V    |
| Overflow drain voltage                  | VOFD                     | -0.5 | -    | +18  | V    |
| Vertical input source voltage           | VISV                     | -0.5 | -    | +18  | V    |
| Horizontal input source voltage         | VISH                     | -0.5 | -    | +18  | V    |
| Overflow gate voltage                   | VOFG                     | -10  | -    | +15  | V    |
| Vertical input gate voltage             | VIG1V, VIG2V             | -10  | -    | +15  | V    |
| Horizontal input gate voltage           | VIG1H, VIG2H             | -10  | -    | +15  | V    |
| Summing gate voltage                    | VSG                      | -10  | -    | +15  | V    |
| Output gate voltage                     | VOG                      | -10  | -    | +15  | V    |
| Reset gate voltage                      | VRG                      | -10  | -    | +15  | V    |
| Transfer gate voltage                   | VTG                      | -10  | -    | +15  | V    |
| Vertical shift register clock voltage   | VP1V, VP2V               | -10  | -    | +15  | V    |
| Horizontal shift register clock voltage | VP1H, VP2H<br>VP3H, VP4H | -10  | -    | +15  | V    |

\*3: Package temperature

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

➤ Operating conditions (MPP mode, Ta=25 °C)

| Parameter                               | Symbol                | S11071 series                |      |      | S10420-01 series |      |      | Unit |
|---|-----------------------|------------------------------|------|------|------------------|------|------|------|
|   |                       | Min.                         | Typ. | Max. | Min.             | Typ. | Max. |      |
| Output transistor drain voltage         | VOD                   | 12                           | 15   | 18   | 23               | 24   | 25   | V    |
| Reset drain voltage                     | VRD                   | 14                           | 15   | 16   | 11               | 12   | 13   | V    |
| Overflow drain voltage                  | VOFD                  | 11                           | 12   | 13   | 11               | 12   | 13   | V    |
| Overflow gate voltage                   | VOFG                  | 0                            | 13   | 14   | 0                | 12   | 13   | V    |
| Output gate voltage                     | VOG                   | 4                            | 5    | 6    | 4                | 5    | 6    | V    |
| Substrate voltage                       | VSS                   | -                            | 0    | -    | -                | 0    | -    | V    |
| Output amplifier return voltage*4       | Vret                  | -                            | 1    | 2    | -                | -    | -    | V    |
| Test point                              | Input source          | VISV, VISH                   | -    | VRD  | -                | -    | -    | V    |
|   | Vertical input gate   | VIG1V, VIG2V                 | -9   | -8   | -                | -9   | -8   | V    |
|   | Horizontal input gate | VIG1H, VIG2H                 | -9   | -8   | -                | -9   | -8   | V    |
| Vertical shift register clock voltage   | High                  | VP1VH, VP2VH                 | 4    | 6    | 8                | 4    | 6    | V    |
|   | Low                   | VP1VL, VP2VL                 | -9   | -8   | -7               | -9   | -8   |      |
| Horizontal shift register clock voltage | High                  | VP1HH, VP2HH<br>VP3HH, VP4HH | 4    | 6    | 8                | 4    | 6    | V    |
|   | Low                   | VP1HL, VP2HL<br>VP3HL, VP4HL | -6   | -5   | -4               | -6   | -5   |      |
| Summing gate voltage                    | High                  | VSGH                         | 4    | 6    | 8                | 4    | 6    | V    |
|   | Low                   | VSGL                         | -6   | -5   | -4               | -6   | -5   |      |
| Reset gate voltage                      | High                  | VRGH                         | 4    | 6    | 8                | 4    | 6    | V    |
|   | Low                   | VRGL                         | -6   | -5   | -4               | -6   | -5   |      |
| Transfer gate voltage                   | High                  | VTGH                         | 4    | 6    | 8                | 4    | 6    | V    |
|   | Low                   | VTGL                         | -9   | -8   | -7               | -9   | -8   |      |
| External load resistance                | RL                    | 2.0                          | 2.2  | 2.4  | 90               | 100  | 110  | kΩ   |

\*4: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.

Electrical characteristics (Ta=25 °C)

| Parameter                             | Symbol                | S11071 series |         |      | S10420-01 series |         |      | Unit |    |
|---------------------------------------|-----------------------|---------------|---------|------|------------------|---------|------|------|----|
|                                       |                       | Min.          | Typ.    | Max. | Min.             | Typ.    | Max. |      |    |
| Signal output frequency*5             | fc                    | -             | 5       | 10   | -                | 0.25    | 0.5  | MHz  |    |
| Vertical shift register capacitance   | -1004(-01)            | CP1V, CP2V    | -       | 200  | -                | -       | 200  | -    | pF |
|                                       | -1006(-01)            |               | -       | 600  | -                | -       | 600  | -    |    |
|                                       | -1104(-01)            |               | -       | 400  | -                | -       | 400  | -    |    |
|                                       | -1106(-01)            |               | -       | 1200 | -                | -       | 1200 | -    |    |
| Horizontal shift register capacitance | -1004(-01)/-1006(-01) | CP1H, CP2H    | -       | 80   | -                | -       | 80   | -    | pF |
|                                       | -1104(-01)/-1106(-01) | CP3H, CP4H    | -       | 160  | -                | -       | 160  | -    |    |
| Summing gate capacitance              | CSG                   | -             | 10      | -    | -                | 10      | -    | pF   |    |
| Reset gate capacitance                | CRG                   | -             | 10      | -    | -                | 10      | -    | pF   |    |
| Transfer gate capacitance             | -1004(-01)/-1006(-01) | CTG           | -       | 30   | -                | -       | 30   | -    | pF |
|                                       | -1104(-01)/-1106(-01) |               | -       | 60   | -                | -       | 60   | -    |    |
| Charge transfer efficiency*6          | CTE                   | 0.99995       | 0.99999 | -    | 0.99995          | 0.99999 | -    | -    |    |
| DC output level*5                     | Vout                  | 7             | 8       | 9    | 17               | 18      | 19   | V    |    |
| Output impedance*5                    | Zo                    | -             | 0.3     | -    | -                | 10      | -    | kΩ   |    |
| Power consumption*5 *7                | P                     | -             | 75      | -    | -                | 4       | -    | mW   |    |

\*5: The values depend on the load resistance. (S11071 series: VOD=15 V, RL=2.2 kΩ, S10420-01 series: VOD=24 V, RL=100 kΩ)

\*6: Charge transfer efficiency per pixel, measured at half of the full well capacity

\*7: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

| Parameter                      | Symbol     | S11071 series |         |      | S10420-01 series                              |         |      | Unit                    |                 |
|--------------------------------|------------|---------------|---------|------|---|---------|------|-------------------------|-----------------|
|                                |            | Min.          | Typ.    | Max. | Min.  | Typ.    | Max. |                         |                 |
| Saturation output voltage      | Vsat       | -             | Fw × CE | -    | -   | Fw × CE | -    | V                       |                 |
| Full well capacity             | Vertical   | Fw            | 50      | 60   | -   | 50      | 60   | -                       | ke <sup>-</sup> |
|                                | Horizontal |               | 150     | 200  | -   | 250     | 300  | -                       |                 |
| Conversion efficiency*8        | CE         | 7             | 8       | 9    | 5.5   | 6.5     | 7.5  | μV/e <sup>-</sup>       |                 |
| Dark current*9                 | DS         | -             | 50      | 500  | -   | 50      | 500  | e <sup>-</sup> /pixel/s |                 |
| Readout noise*10               | Nread      | -             | 23      | 28   | -   | 6       | 15   | e <sup>-</sup> rms      |                 |
| Dynamic range*11               | Drange     | 6520          | 8700    | -    | 41700   | 50000   | -    | -                       |                 |
| Spectral response range        | λ          | 200 to 1100   |         |      | 200 to 1100<br>120 to 1100 (S10420-1106NW-01) |         |      | nm                      |                 |
| Photoresponse nonuniformity*12 | PRNU       | -             | ±3      | ±10  | -   | ±3      | ±10  | %                       |                 |

\*8: The values depend on the load resistance. (S11071 series: VOD=15 V, RL=2.2 kΩ, S10420-01 series: VOD=24 V, RL=100 kΩ)

\*9: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.

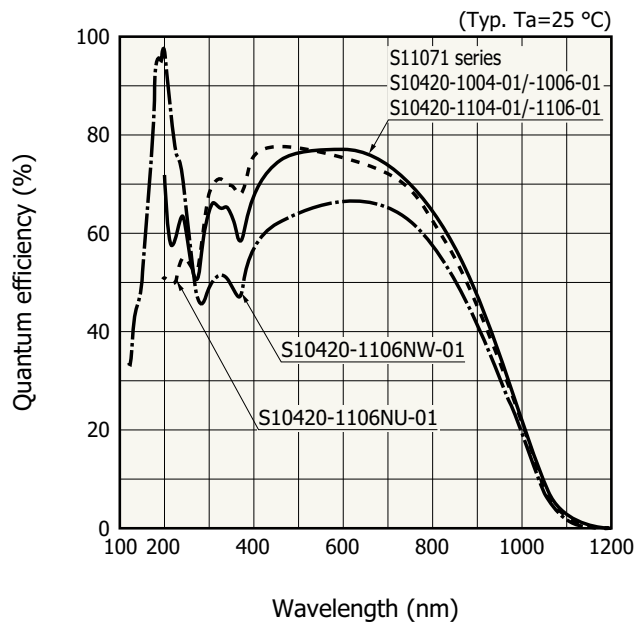
\*10: S11071 series (temperature: 25 °C): fc=2 MHz, S10420-01 series (temperature: -40 °C): fc=20 kHz

\*11: Dynamic range = Full well capacity / Readout noise

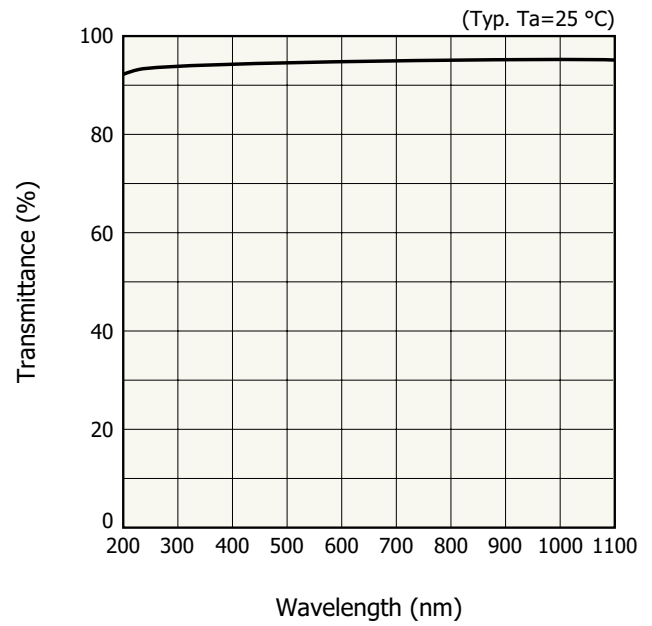
\*12: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \text{ [%]}$$

**Spectral response (typical example, without window)\*13**

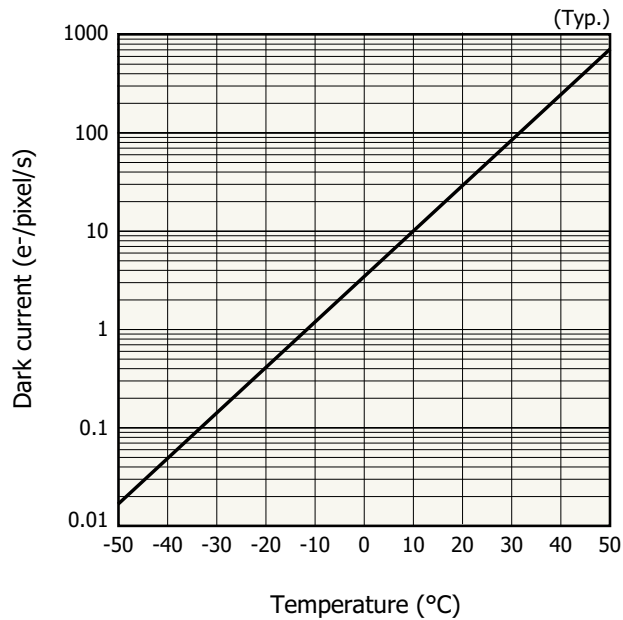


**Spectral transmittance characteristic of window material**



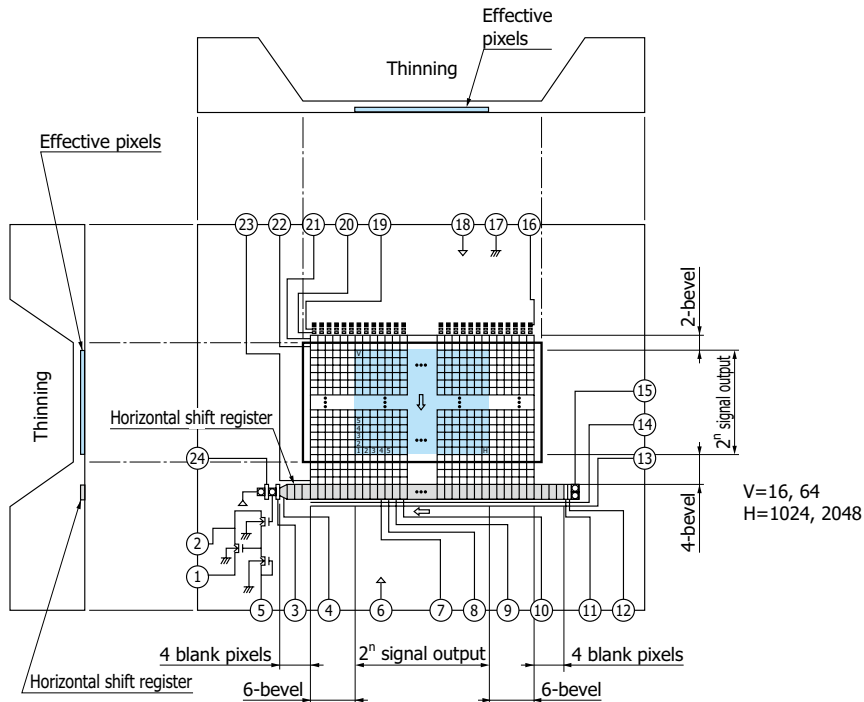
\*13: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

**Dark current vs. temperature**



Device structure (conceptual drawing of top view in dimensional outline)

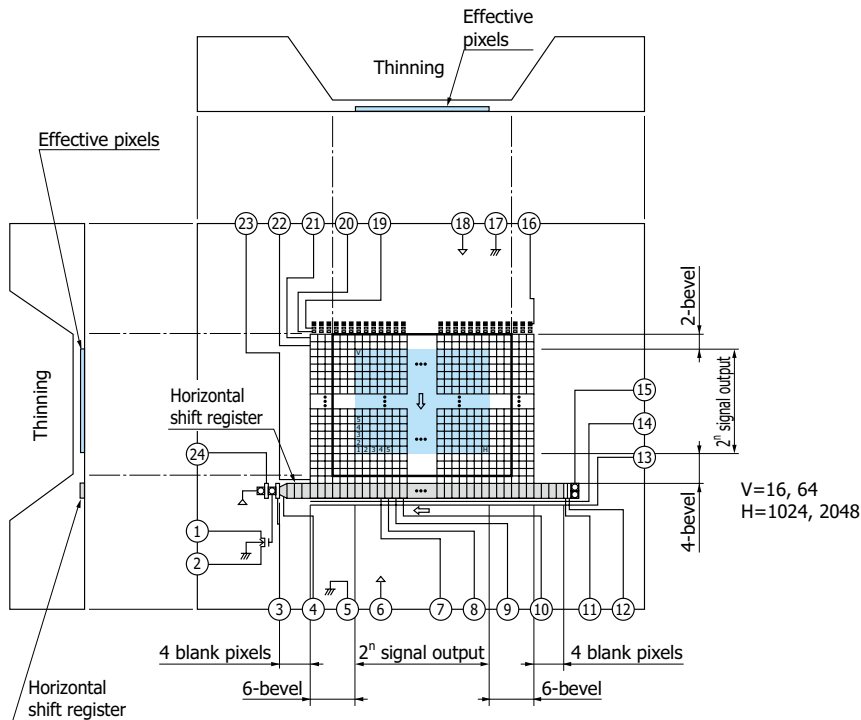
S11071 series



Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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S10420-01 series



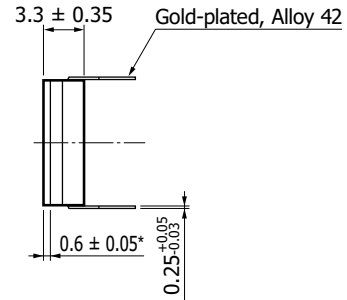
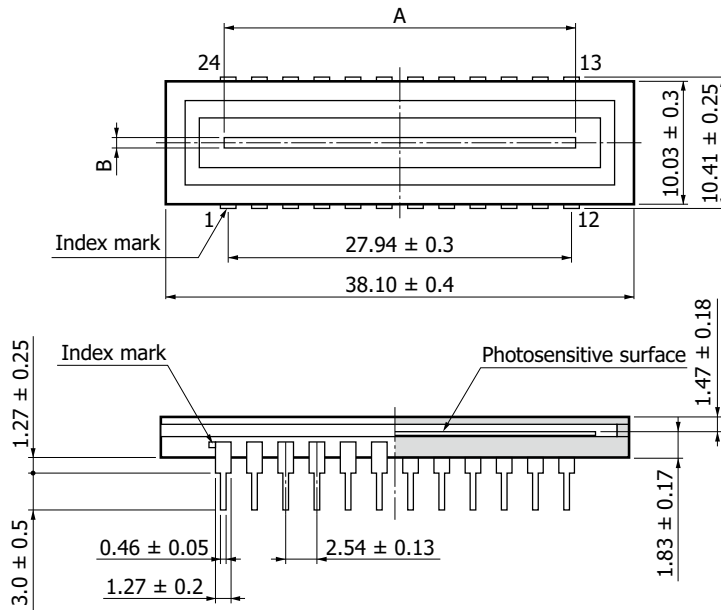
Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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**Dimensional outline (unit: mm)**

S11071 series, S10420-1004-01/-1006-01/-1104-01/-1106-01

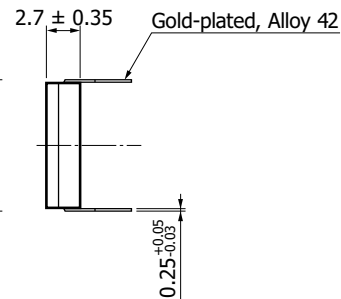
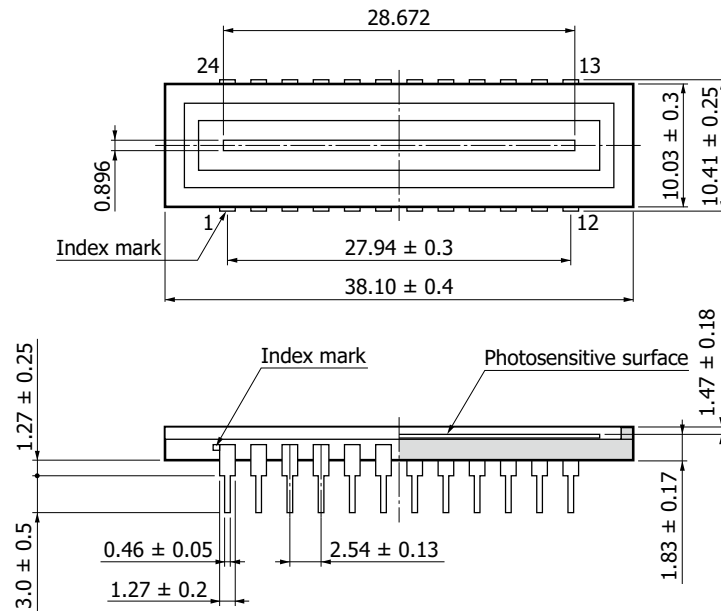


| Type no.          | Photosensitive area |                      |
|-------------------|---------------------|----------------------|
|                   | A                   | B                    |
| S11071/<br>S10420 | -1004(-01)          | 14.336 (H) 0.224 (V) |
|                   | -1006(-01)          | 14.336 (H) 0.896 (V) |
|                   | -1104(-01)          | 28.672 (H) 0.224 (V) |
|                   | -1106(-01)          | 28.672 (H) 0.896 (V) |

\* Glass thickness (refractive index≈1.5)

KMPDA0223EF

S10420-1106NU-01/-1106NW-01



KMPDA0627EA



Pin connections

| S11071 series |        |                                      |                             |
|---------------|--------|--------------------------------------|-----------------------------|
| Pin no.       | Symbol | Function                             | Remark (standard operation) |
| 1             | OS     | Output transistor source             | RL=2.2 kΩ                   |
| 2             | OD     | Output transistor drain              | +15 V                       |
| 3             | OG     | Output gate                          | +5 V                        |
| 4             | SG     | Summing gate                         | Same pulse as P4H           |
| 5             | Vret   | Output amplifier return              | +1 V                        |
| 6             | RD     | Reset drain                          | +15 V                       |
| 7             | P4H    | CCD horizontal register clock-4      |                             |
| 8             | P3H    | CCD horizontal register clock-3      |                             |
| 9             | P2H    | CCD horizontal register clock-2      |                             |
| 10            | P1H    | CCD horizontal register clock-1      |                             |
| 11            | IG2H   | Test point (horizontal input gate-2) | -8 V                        |
| 12            | IG1H   | Test point (horizontal input gate-1) | -8 V                        |
| 13            | OFG    | Over flow gate                       | +13 V                       |
| 14            | OFD    | Over flow drain                      | +12 V                       |
| 15            | ISH    | Test point (horizontal input source) | Connect to RD               |
| 16            | ISV    | Test point (vertical input source)   | Connect to RD               |
| 17            | SS     | Substrate                            | GND                         |
| 18            | RD     | Reset drain                          | +15 V                       |
| 19            | IG2V   | Test point (vertical input gate-2)   | -8 V                        |
| 20            | IG1V   | Test point (vertical input gate-1)   | -8 V                        |
| 21            | P2V    | CCD vertical register clock-2        |                             |
| 22            | P1V    | CCD vertical register clock-1        |                             |
| 23            | TG     | Transfer gate                        | Same pulse as P2V           |
| 24            | RG     | Reset gate                           |                             |

| S10420-01 series |        |                                      |                             |
|------------------|--------|--------------------------------------|-----------------------------|
| Pin no.          | Symbol | Function                             | Remark (standard operation) |
| 1                | OS     | Output transistor source             | RL=100 kΩ                   |
| 2                | OD     | Output transistor drain              | +24 V                       |
| 3                | OG     | Output gate                          | +5 V                        |
| 4                | SG     | Summing gate                         | Same pulse as P4H           |
| 5                | SS     | Substrate                            | GND                         |
| 6                | RD     | Reset drain                          | +12 V                       |
| 7                | P4H    | CCD horizontal register clock-4      |                             |
| 8                | P3H    | CCD horizontal register clock-3      |                             |
| 9                | P2H    | CCD horizontal register clock-2      |                             |
| 10               | P1H    | CCD horizontal register clock-1      |                             |
| 11               | IG2H   | Test point (horizontal input gate-2) | -8 V                        |
| 12               | IG1H   | Test point (horizontal input gate-1) | -8 V                        |
| 13               | OFG    | Over flow gate                       | +12 V                       |
| 14               | OFD    | Over flow drain                      | +12 V                       |
| 15               | ISH    | Test point (horizontal input source) | Connect to RD               |
| 16               | ISV    | Test point (vertical input source)   | Connect to RD               |
| 17               | SS     | Substrate                            | GND                         |
| 18               | RD     | Reset drain                          | +12 V                       |
| 19               | IG2V   | Test point (vertical input gate-2)   | -8 V                        |
| 20               | IG1V   | Test point (vertical input gate-1)   | -8 V                        |
| 21               | P2V    | CCD vertical register clock-2        |                             |
| 22               | P1V    | CCD vertical register clock-1        |                             |
| 23               | TG     | Transfer gate                        | Same pulse as P2V           |
| 24               | RG     | Reset gate                           |                             |

### Precautions (electrostatic countermeasures)

■ Electrostatic countermeasures

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Handling the temporary window type (S10420-1106NU-01/-1106NW-01)

- Never touch or wipe the photosensitive surface. It will adversely affect the characteristics.

### Related information

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

■ Precautions

- Disclaimer
- Image sensors
- Unsealed products

■ Technical information

- FFT-CCD area image sensor

### Driver circuits for CCD image sensor C11287-01/C11288-01 [sold separately]

The C11287-01, C11288-01 are driver circuits designed for HAMAMATSU CCD image sensors. The C11287-01 is for S10420-01 series, S16010 series and S14650 series. The C11288-01 is for S11071 series and S14660 series. The C11287-01, C11288-01 can be used in spectrometers, etc. when combined with the CCD image sensor.

### Features

- **Built-in 16-bit A/D converter**
- **Interface to computer: USB 2.0**
- **Power supply: USB bus power operation (C11287-01)  
DC+5 V operation (C11288-01)**



C11287-01/C11288-01

Information described in this material is current as of September 2021.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use. Copying or reprinting the contents described in this material in whole or in part is prohibited without our prior permission.

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